WHAT IS CLAIMED IS:

1. An integrated circuit structure comprising:

an isolation structure that electrically isolates an active region of an integrated circuit substrate from adjacent active regions;

an insulation layer extending from the isolation structure to beneath the active region; and

an epitaxial silicon layer that extends from the active region through the insulation layer to a substrate beneath the insulation layer.

2. An integrated circuit structure according to Claim 1 wherein the insulation layer comprises a trench thermal oxide layer on an inner wall of a trench in the substrate, the insulation layer extending though the inner wall of the trench to beneath the active region.

3. An integrated circuit structure according to Claim 2 wherein the isolation structure further comprises:

a nitride liner on the trench thermal oxide layer;

a field oxide layer in the trench on the nitride liner.

4. An integrated circuit structure according to Claim 3 wherein the nitride liner extends through the inner wall into the insulation layer beneath the active region.

5. An integrated circuit structure according to Claim 1 further comprising:

an impurity-doped region at an interface of the substrate and the epitaxial silicon layer.

6. An integrated circuit structure according to Claim 1 wherein the insulation layer comprises a thermal oxide.

7. An integrated circuit structure according to Claim 1 wherein the active region comprises a strained silicon crystalline structure.

8. An integrated circuit structure according to Claim 2 wherein the epitaxial silicon layer comprises a first epitaxial silicon layer in the active region adjacent to and in contact with the inner wall of the trench, the structure further comprising:

a second epitaxial silicon layer in the active region spaced apart from the first epitaxial silicon layer.

9. A method of forming an integrated circuit structure comprising:

forming an epitaxial silicon layer from an active region through a silicon layer having a strained crystalline structure to a substrate beneath the silicon layer; and then

replacing the silicon layer with an insulation layer.

10. A method according to Claim 9 wherein the silicon layer comprises a silicon germanium layer.

11. A method according to Claim 9 wherein the step of replacing comprises:

removing the silicon layer having the strained crystalline structure from beneath the active region to form a gap between the active region and the substrate; and

forming the insulation layer in the gap.

12. A method according to Claim 9 wherein the silicon layer comprises a first silicon layer and the insulation layer comprises a first insulation layer, wherein the step of forming further comprises:

forming the epitaxial silicon layer from the active region through the first silicon layer and a spaced apart second silicon layer beneath the first silicon layer having a strained crystalline structure to the substrate beneath the second silicon layer; and

the step of replacing comprises replacing the first and second silicon layers with the first insulation layer and a second insulation layer respectively.

13. A method according to Claim 12 wherein the step of forming the insulation layer in the gap further comprises:

forming an isolation structure that electrically isolates the active region from adjacent active regions, wherein the isolation structure includes an inner wall that contacts the active region.

14. A method according to Claim 13 wherein step of forming the epitaxial silicon layer comprises further comprises:

forming first and second spaced apart epitaxial silicon layers from the active region through the silicon layer to the substrate beneath the silicon layer, wherein the first epitaxial silicon layer contacts the inner wall and the second epitaxial silicon layer is spaced apart from the inner wall.

15. A method of forming an integrated circuit structure comprising:

forming a silicon layer having a strained crystalline structure beneath an active region of an integrated circuit;

forming an epitaxial silicon layer from the active region through the silicon layer to a substrate beneath the silicon layer;

removing the silicon layer from between the active region and the substrate to form a gap; and

forming an insulating layer in the gap.

16. A method of forming a semiconductor device, comprising:

sequentially forming at least one pair of a sacrificial layer and a silicon layer on a semiconductor substrate;

forming an opening exposing the semiconductor substrate by sequentially patterning a predetermined region of at least one pair of the sacrificial layer and the silicon layer;

selectively growing an epitaxial layer from the exposed semiconductor substrate in the opening, thereby filling the opening;

forming a trench for forming a field oxide layer by sequentially patterning at least one pair of the sacrificial layer and the silicon layer and an upper part of the semiconductor substrate;

removing the sacrificial layer;

forming a trench thermal oxide layer at an inner wall and a bottom of the trench and simultaneously forming an insulation layer along a region where the

sacrificial layer is removed, by thermally oxidizing the semiconductor substrate;

forming a nitride liner on the trench oxide layer; and

filling the trench by stacking a field oxide layer on the nitride liner.

17. The method as claimed in claim 16, wherein the insulation layer is conformally formed along a region where the sacrificial layer is removed, and the nitride liner is simultaneously formed on a surface of the insulation layer when the nitride liner is formed on the trench thermal oxide layer.

18. The method as claimed in claim 16, wherein the sacrificial layer is formed of silicon germanium (SiGe).

19. The method as claimed in claim 16, wherein the removing of the sacrificial layer is performed by using plasma of at least one gas selected from a group consisting of hydrogen (H_2), oxygen (O_2), nitrogen (N_2) and fluoric compounds such as NF_3 and CF_4.

20. The method as claimed in claim 16, wherein the removing of the sacrificial layer is performed by using at least one solution selected from a group consisting of ammonia water (NH_4OH), hydrogen peroxide (H_2O_2), deionized water (H_2O), nitric acid (HNO_3) and fluoric acid (HF).

21. The method as claimed in claim 16, after forming the opening, further comprising an impurity-doped region into the semiconductor substrate under the opening.